REMARKS

This application has been carefully reviewed in light of the Office Action dated November 20, 2003. Claims 1, 2 and 5 to 7 remain pending in the application, with Claims 3 and 4 having been canceled and Claims 1 and 6, the independent claims herein, having been amended. Reconsideration and further examination are respectfully requested.

Claims 1, 3 and 6 were objected to for informalities that have been attended to by amendment or cancellation of the claims as recited above. Withdrawal of the objections is respectfully requested.

Claims 1 and 2 were rejected under 35 U.S.C. § 102(b) over Japan 61-206286 (Kazuo), Claims 3 to 5 were rejected under 35 U.S.C. § 103(a) over Kazuo in view of U.S. Patent No. 6,034,982 (Iwase), and Claims 6 and 7 were rejected under § 103(a) over Japan 10-48557 (Nakanishi) in view of Kazuo. Reconsideration and withdrawal of the rejections are respectfully requested.

The present invention concerns semiconductor arrays. Conventionally, a chip having a plurality of luminous spots is soldered to a mount by soldering the chip near the luminous spots. Because the mount and the chip are generally made of different materials that have different heat expansion rates, one material (generally the mount) cools faster than the other (generally the chip), thereby inducing residual stresses near the soldered area when the materials cool after soldering. The residual stresses near the luminous spot cause a polarization angle difference between the spots, which in turn results in a sub-scanning pitch error. Thus, the greater the residual stress, the greater the polarization angle difference and the greater the sub-scanning pitch error.

The present invention addresses the foregoing by soldering the chip to the mount while the chip projects from a corresponding end facet of the mount with a side of

the chip having the plurality of luminous spots projecting away from the corresponding end facet of said mount. Thus, as seen in Figure 1, when the chip is soldered to the mount, the luminous spots are further away from the soldered area, thereby reducing the residual stress near the luminous spots. As a result, the polarization angle difference between the luminous spots is reduced, thereby reducing the sub-scanning pitch error.

With specific reference to the claims, amended independent Claim 1 is a semiconductor laser array comprising a chip having a plurality of luminous spots, and a mount for mounting the chip by means of solder, wherein, semiconductor lasers of the semiconductor laser array are buried heterojunction type lasers, and wherein the chip is soldered to the mount in a fashion of junction down while the chip projects from a corresponding end facet of the mount with a side of the chip having the plurality of luminous spots projecting away from the corresponding end facet of said mount.

Amended independent Claim 6 is an optical scanner claim that includes features substantially corresponding to those of Claim 1.

The applied art, alone or in any permissible combination, is not seen to disclose or to suggest the features of Claims 1 and 6, and in particular is not seen to disclose or to suggest at least the feature of soldering a chip to the mount in a fashion of junction down while the chip projects from a corresponding end facet of the mount with a side of the chip having a plurality of luminous spots projecting away from the corresponding end facet of said mount.

Kazuo is merely seen to disclose bonding a laser chip 9 onto a semiconductor wafer 1 such that a laser beam emitting end facet 11 projects into a groove of the wafer 1. However, Kazuo is not seen to disclose or to suggest at least the feature of soldering a chip to the mount in a fashion of junction down while the chip projects from a

corresponding end facet of the mount with a side of the chip having a plurality of luminous spots projecting away from the corresponding end facet of said mount.

Nakanishi merely discloses deflecting laser light by a rotating polygon mirror so that an image is formed on a photoreceptor through a plastic lens. However, Nakanishi is not believed to disclose or to suggest at least the feature of soldering a chip to the mount in a fashion of junction down while the chip projects from a corresponding end facet of the mount with a side of the chip having a plurality of luminous spots projecting away from the corresponding end facet of said mount.

Iwase is merely seen to disclose a semiconductor laser array mounted to a sub-mount by soldering the array flush with the end facet of the sub-mount. However, when this arrangement is soldered, it suffers from the problems described above since the soldering occurs very near the luminous spots. Thus, Iwase is also not seen to disclose or to suggest at least the feature of soldering a chip to the mount in a fashion of junction down while the chip projects from a corresponding end facet of the mount with a side of the chip having a plurality of luminous spots projecting away from the corresponding end facet of said mount.

In view of the foregoing amendments and remarks, all of Claims 1, 2 and 5 to 7 are believed to be allowable.

No other matters having been raised, the entire application is believed to be in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience.

Applicants' undersigned attorney may be reached in our Costa Mesa, California, office by telephone at (714) 540-8700. All correspondence should be directed to our address given below.

Respectfully submitted,

Attorney for Applicants

Registration No. 42,746

FITZPATRICK, CELLA, HARPER & SCINTO
30 Rockefeller Plaza
New York, New York 10112-2200
Facsimile: (212) 218-2200

CA_MAIN 76874 v 1